WHAT IS CLAIMED IS:

1. A nonvolatile memory array, comprising:

an array of nonvolatile memory devices;

at least one driver circuit; and

a substrate;

wherein the at least one driver circuit is not located in a bulk monocrystalline silicon substrate.

2. The array of claim 1, wherein the at least one driver circuit is located in a silicon on insulator substrate.

3. The array of claim 2, wherein the at least one driver circuit is located in a single crystal silicon layer over a silicon oxide layer formed by a SIMOX method.

4. The array of claim 2, wherein the at least one driver circuit is located in a single crystal silicon layer over an insulating layer formed by a seeded lateral epitaxy method.

5. The array of claim 2, wherein the at least one driver circuit is located in a single crystal silicon layer over an insulating substrate formed by a wafer bonding method.

6. The array of claim 2, wherein:

the at least one driver circuit is located in a polycrystalline silicon layer;

the polycrystalline silicon layer is located over an insulating layer; and

the insulating layer is located over a bulk monocrystalline silicon substrate.

7. The array of claim 2, wherein the at least one driver circuit is located above a monocrystalline silicon substrate.

8. The array of claim 7, wherein the at least one driver circuit is separated from the monocrystalline silicon substrate by an insulating layer.

9. The array of claim 2, wherein the at least one driver circuit is formed above a glass substrate.

10. The array of claim 2, wherein the at least one driver circuit is formed above a plastic substrate.

11. The array of claim 2, wherein the at least one driver circuit is formed above a ceramic substrate.

12. The array of claim 11, wherein the at least one driver circuit is formed in a single crystal silicon layer formed on a sapphire substrate.

13. The array of claim 1, wherein the at least one driver circuit is formed in a III-V, II-VI or IV-IV semiconductor substrate.

14. The array of claim 13, wherein the at least one driver circuit is formed in a GaAs substrate.

15. The array of claim 1, wherein the at least one driver circuit comprises a decoding circuit, a sensing circuit and a programming circuit.

16. The array of claim 1, wherein the at least one driver circuit comprises a plurality of CMOS thin film transistors.

17. The array of claim 16, wherein each CMOS thin film transistors comprise:

a gate electrode;

a first insulating layer adjacent to a first side of the gate electrode;

a first semiconductor layer having a first conductivity type disposed on a side of the first insulating layer opposite to the gate electrode;

first source and drain regions of a second conductivity type disposed in the first semiconductor layer;

first source and drain electrodes in contact with the first source and drain regions and disposed on a side of the first semiconductor layer opposite to the first insulating layer;

a second insulating layer adjacent to a second side of the gate electrode;

a second semiconductor layer having a second conductivity type disposed on a side of the second insulating layer opposite to the gate electrode;

second source and drain regions of a first conductivity type disposed in the second semiconductor layer; and

second source and drain electrodes in contact with the second source and drain regions and disposed on a side of the second semiconductor layer opposite to the second insulating layer.

18. The array of claim 17, further comprising:

a first charge storage region which includes the first insulating layer; and

a second charge storage region which includes the second insulating layer.

19. The array of claim 1, wherein the array of nonvolatile memory devices comprises an array of PROMs, EPROMs or EEPROMs.

20. The array of claim 19, wherein the array of nonvolatile memory devices comprises a monolithic three dimensional array of memory devices.

21. The array of claim 20, wherein the array of nonvolatile memory devices comprises a three dimensional array of antifuses.

22. The array of claim 21, wherein the array of antifuses comprise a first set of rail stack conductors, a second set of rail stack conductors extending in a different direction than the first set of rail stack conductors, and an insulating layer disposed between the first and the second sets of rail stacks.

23. The array of claim 22, further comprising semiconductor diodes located at intersections of the conductors of the first and the second sets of rail stacks.

24. The array of claim 23, wherein the diodes comprise P+ / N- diodes.

25. The array of claim 20, wherein the array comprises:

a first plurality of spaced-apart conductors disposed at a first height above the substrate in a first direction; and

a second plurality of spaced-apart rail-stacks disposed above the first height in a second direction different from the first direction, each rail-stack including a semiconductor film of a first conductivity type in contact with said first plurality of spaced-apart conductors, a local charge

storage film disposed above the semiconductor film and a conductive film disposed above the local charge storage film.

26. The array of claim 25, wherein:

a space between said spaced-apart conductors contains a planarized deposited oxide material;

said semiconductor film comprises polysilicon; and

said local charge storage film is selected from a group consisting of a dielectric isolated floating gate, an ONO dielectric film and an insulating layer containing conductive nanocrystals.

27. The array of claim 20, wherein each device of the three dimensional array comprises:

a first conductor;

a second conductor; and

a pillar vertically disposed between the first and the second conductors;

wherein the pillar comprises:

a semiconductor diode having a first conductivity type region and a second conductivity type region;

a tunneling oxide;

a charge storage region; and

a blocking oxide.

28. The array of claim 20, wherein each memory device of the three dimensional array comprises:

a source region, a channel region and a drain region each vertically aligned with one another to form a pillar;

a first electrode contacting the source region;

a second electrode contacting the drain regions;

a charge storage region located adjacent to and in contact with the channel region; and

a control gate located adjacent to and in direct contact with the charge storage region.

29. The array of claim 20, wherein the array of nonvolatile memory devices comprises an array of TFT EEPROMs.

30. The array of claim 29, wherein the array comprises:

a plurality of vertically separated device levels, each level comprising an array of TFT EEPROMs, each TFT EEPROM comprising a channel, source and drain regions, a control gate, and a charge storage region between the channel and the control gate;

a plurality of bit line columns in each device level, each bit line contacting the source or the drain regions of the TFT EEPROMs;

a plurality of word line rows in each device level; and

at least one interlayer insulating layer located between the device levels.

31. The array of claim 30, wherein:

the channel of each TFT EEPROM comprises amorphous silicon or polysilicon;

the columns of bit lines extend substantially perpendicular to a source-channel-drain direction of the TFT EEPROMs;

each word line contacts the control gates of the TFT EEPROMs, and the rows of word lines extend substantially parallel to the source-channel-drain direction of the TFT EEPROMs; and

the word lines are self aligned to the control gates of the array of TFT EEPROMs and the word lines are self aligned to the channel and the

charge storage regions of the TFT EEPROMs located below the respective word lines.

32. The array of claim 27, wherein each charge storage region comprises:

an ONO dielectric film;

an insulating layer containing conductive nanocrystals; or

an isolated floating gate comprising:

a tunnel dielectric above the channel;

the floating gate above the tunnel dielectric; and

a control gate dielectric above the floating gate.

33. The array of claim 20, wherein the array of nonvolatile memory devices comprises a flash memory array which is programmed by FN tunneling.

34. The array of claim 33, wherein the array comprises:

a first plurality of spaced-apart conductive bit lines disposed at a first height above the substrate in a first direction; and

a second plurality of spaced-apart rail-stacks disposed at a second height in a second direction different from the first direction, each rail-stack including a plurality of semiconductor islands whose first surface is in contact with said first plurality of spaced-apart conductive bit lines, a conductive word line, and charge storage regions disposed between a second surface of the semiconductor islands and the word line.

35. The array of claim 1, further comprising at least one optoelectronic component formed over the substrate.

36. The array of claim 35, wherein:

the at least one driver circuit is formed in a III-V substrate or above a glass, plastic or ceramic substrate; and

the at least one optoelectronic component comprises a laser, an LED or a photodetector.

37. The array of claim 1, further comprising at least one microwave or radio frequency circuit formed over the substrate which comprises a III-V semiconductor substrate.

38. The array of claim 1, further comprising a liquid crystal display formed above the substrate.

39. The array of claim 38, wherein the at least one driver circuit is formed above a glass, plastic or ceramic substrate.

40. The array of claim 1, further comprising a smart card circuit formed over the substrate which comprises a plastic substrate.

41. A nonvolatile memory array, comprising:

a monocrystalline silicon substrate;

at least one driver circuit formed above the substrate; and

an array of nonvolatile memory devices formed above the substrate.

42. The array of claim 41, wherein the at least one driver circuit is separated from the monocrystalline silicon substrate by an insulating layer.

43. The array of claim 41, wherein the at least one driver circuit comprises a decoding circuit, a sensing circuit and a programming circuit.

44. The array of claim 41, wherein the array of nonvolatile memory devices comprises an array of EPROMs.

45. The array of claim 41, wherein the array of nonvolatile memory devices comprises a monolithic three dimensional array of memory devices.

46. The array of claim 45, wherein the array of nonvolatile memory devices comprises a three dimensional array of antifuses.

47. The array of claim 46, wherein the array of antifuses comprise a first set of rail stack conductors, a second set of rail stack conductors extending in a different direction than the first set of rail stack conductors, and an insulating layer disposed between the first and the second sets of rail stacks.

48. The array of claim 47, further comprising semiconductor diodes located at intersections of the conductors of the first and the second sets of rail stacks.

49. The array of claim 48, wherein the diodes comprise P+ / N- diodes.

50. A method of making a nonvolatile memory array, comprising:

forming at least one driver circuit above a substrate or in a semiconductor substrate other than a monocrystalline silicon substrate; and

forming an array of nonvolatile memory devices.

51. The method of claim 50, wherein the at least one driver circuit is formed in a silicon on insulator substrate.

52. The method of claim 51, further comprising:
providing a monocrystalline silicon substrate;
implanting oxygen into the substrate;
annealing the substrate to form a silicon oxide layer in the substrate such that a single crystal silicon layer remains above the silicon oxide layer; and
forming the at least one driver circuit in the single crystal silicon layer.

53. The method of claim 51, further comprising:
providing a monocrystalline silicon substrate;
forming a silicon oxide layer over the substrate;
forming a single crystal silicon layer over the silicon oxide layer using the substrate as a seed; and
forming the at least one driver circuit in the single crystal silicon layer.

54. The method of claim 51, further comprising:
providing a monocrystalline silicon substrate;
forming a silicon oxide layer over the substrate;
forming a polysilicon layer over the silicon oxide; and
forming the at least one driver circuit in the polysilicon layer.

55. The method of claim 51, further comprising:
providing a temporary monocrystalline silicon substrate;
forming the at least one driver circuit in the temporary substrate;
selectively removing the temporary substrate; and

attaching a permanent substrate to the at least one driver circuit.

56. The method of claim 50, wherein the at least one driver circuit is formed above a monocrystalline silicon substrate.

57. The method of claim 56, further comprising forming an interlayer insulating layer over the substrate prior to forming the at least one driver circuit.

58. The method of claim 50, wherein the at least one driver circuit is formed above a glass, plastic or ceramic substrate.

59. The method of claim 50, wherein the at least one driver circuit is formed in a III-V, II-VI or IV-IV semiconductor substrate.

60. The method of claim 50, wherein the at least one driver circuit comprises a decoding circuit, a sensing circuit and a programming circuit.

61. The method of claim 50, further comprising forming a first interlayer insulating layer over the at least one driver circuit.

62. The method of claim 61, wherein the step of forming the array of nonvolatile memory devices comprises depositing at least one first semiconductor layer over the first interlayer insulating layer and forming a first array of PROMs, EPROMs or EEPROMs in the at least one first semiconductor layer.

63. The method of claim 62, further comprising:

forming a second interlayer insulating layer over the array of PROMs, EPROMs or EEPROMs;

depositing at least one second semiconductor layer over the second interlayer insulating layer; and

forming a second array of PROMs, EPROMs or EEPROMs in the at least one second semiconductor layer.

64. The method of claim 63, wherein the first array of PROMs, EPROMs or EEPROMs comprises at least one array selected from an array of rail stack antifuses, an array of rail stack EEPROMs, an array of two terminal pillar memory devices, an array of pillar EEPROMs, and an array of TFT EEPROMs.

65. The method of claim 50, further comprising depositing a semiconductor layer over the substrate and forming an additional device in the deposited layer.

66. The method of claim 65, wherein the additional device is selected from a group consisting of an optoelectronic device, a microwave circuit, a radio frequency circuit, a liquid crystal display and a smart card circuit.

67. The method of claim 66, further comprising forming a liquid crystal display TFT at the same time as forming a memory driver circuit TFT or a memory array TFT.

68. The method of claim 50, where the step of forming at least one driver circuit comprises:

providing a circuit comprising a plurality of charge storage devices;

applying a first programming voltage to a first set of charge storage devices to turn the first set of charge storage devices off by increasing a threshold voltage of the first set of charge storage devices; and

applying a second programming voltage to a second set of charge storage devices to form a conductive link through a charge storage region of the second set of charge storage devices to convert the second set of charge storage devices to antifuse devices.